WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

an electrically data rewritable non-volatile semiconductor memory cell; and

a write circuit configured to write data in said memory cell, said write circuit writes a data in said memory cells by supplying a write voltage and a write control voltage to said memory cell, continues the writing of said data in said memory cell by changing the supply of said write control voltage to said memory cell in response to an advent of a first write state of said memory cell and inhibits any operation of writing a data to said memory cell by further changing the supply of said write control voltage to said memory cell in response to an advent of a second write state of said memory cell.

2. The device according to claim 1, wherein said memory cell stores an n-valued data (where n represents a positive integer not smaller than 3).

3. The device according to claim 1, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage.

4. The device according to claim 1, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage so as to make it increase stepwise.

5. The device according to claim 1, wherein said memory cell is a non-volatile transistor having a floating gate, a control gate, a source and a drain; and

said write circuit supplies said write voltage to the control gate of said non-volatile transistor and said write control voltage to the drain of said non-volatile transistor.

6. A non-volatile semiconductor memory device comprising:

an electrically data rewritable non-volatile semiconductor memory cell; and

a write circuit configured to write data in said memory cell, said write circuit writes a data in said memory cells by supplying a write voltage and a write control voltage having a first value to said memory cell, continues the writing of said data in said memory cell by changing said write control voltage to a second value different from said first value in response to an advent of a first write state of said memory cell and inhibits any operation of writing a data to said memory cell by further changing said write control voltage to a third value different from said first and second values in response to an advent of a second write state of said memory cell.

7. The device according to claim 6, wherein said second value is greater than said first value

and said third value is greater than said second value.

8. The device according to claim 7, wherein said third value is the value of the supply voltage.

9. The device according to claim 6, wherein said memory cell stores an n-valued data (where n represents a positive integer not smaller than 3).

10. The device according to claim 6, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage.

11. The device according to claim 6, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage so as to make it increase stepwise at a predetermined rate.

12. The device according to claim 6, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage so as to make it increase stepwise at a constant rate.

13. The device according to claim 6, wherein said memory cell is a non-volatile transistor having a floating gate, a control gate, a source and a drain; and

said write circuit supplies said write voltage to the control gate of said non-volatile transistor and said write control voltage to the drain of said non-volatile transistor.

14. A non-volatile semiconductor memory device

comprising:

an electrically data rewritable non-volatile semiconductor memory cell; and

a write circuit configured to write data in said memory cell, said write circuit writes a data in said memory cells by supplying a write voltage and a write control voltage having a first value to said memory cell for a first time period while supplying a write voltage to said memory cell, continues the writing of said data in said memory cell by supplying said write control voltage having a first value for a second time period different for said first time period while supplying said write voltage to said memory cell in response to an advent of a first write state of said memory cell and inhibits any operation of writing a data to said memory cell by changing said write control voltage to a second value different from said first value in response to an advent of a second write state of said memory cell.

15. The device according to claim 14, wherein said second time period is shorter than said first time period and said second value is greater than said first value.

16. The device according to claim 14, wherein said second value is the value of the supply voltage.

17. The device according to claim 14, wherein

said memory cell stores an n-valued data (where n represents a positive integer not smaller than 3).

18. The device according to claim 14, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage.

19. The device according to claim 14, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage so as to make it increase stepwise.

20. The device according to claim 14, wherein said write circuit writes a data into said memory cell by changing the level of said write voltage so as to make it increase stepwise at a constant rate.

21. The device according to claim 14, wherein said memory cell is a non-volatile transistor having a floating gate, a control gate, a source and a drain; and

said write circuit supplies said write voltage to the control gate of said non-volatile transistor and said write control voltage to the drain of said non-volatile transistor.

22. A non-volatile semiconductor memory device comprising:

a plurality of electrically data rewritable non-volatile semiconductor memory cells;

a plurality of word lines commonly connected to said plurality of memory cells;

a plurality of bit lines connected respectively to said plurality of memory cells; and

a write circuit configured to write data in said memory cells by supplying a write voltage and a write control voltage to said plurality of memory cells;

wherein said write circuit has data storage circuits for storing first and second control data, said storage circuits being arranged in correspondence to said plurality of bit lines;

said write circuit stores the first control data in said data storage circuit according to the data to be written into corresponding memory cells, writes data into corresponding memory cells by supplying a write voltage to said word lines and a write control voltage to a bit line corresponding to said data storage circuit storing data to be written as the first control data, stores as the second control data a data indicating the termination of a first write state in the data storage circuit corresponding to the memory cell already in the first write state out of said memory cells in operation of writing data, subsequently writes a data into said memory cell already in the first write state by changing the supply of said write control voltage, stores as first control data a data indicating the termination of a second write state in said data storage circuit corresponding to the memory cell already in the second write state out of said

memory cells in operation of writing data and subsequently inhibits any operation of writing data to said memory cells already in said second write state.

23. The device according to claim 22, wherein said write circuit stores the data indicating the termination of a first write state in said data storage circuit as said second control data and subsequently causes it to hold the data.

24. The device according to claim 22, wherein said write circuit stores as said second control data a data indicating the termination of the first write state in said data storage circuit and subsequently writes said data in said memory cells already in said first write state, changing the value of said write control voltage.

25. The device according to claim 22, wherein said write circuit stores as said second control data a data indicating the termination of the first write state in said data storage circuit and subsequently writes said data in said memory cells already in said first write state, changing the time period of supplying said write control voltage.

26. A non-volatile semiconductor memory device comprising:

an electrically data rewritable non-volatile semiconductor memory cell; and

a write circuit configured to write data in said

memory cell, said write circuit writes a data in said memory cell by supplying a sequentially stepwise increasing write voltage and a write control voltage having a first effective voltage level to said memory cell, continues the writing of said data in said memory cell by changing the supply of said write control voltage to said memory cell to a second effective voltage different from said first effective voltage in response to an advent of a first write state of said memory cell and inhibits any operation of writing a data to said memory cell by further changing the supply of said write control voltage to said memory cell in response to the advent of a second write state of said memory cell.

27. The device according to claim 26, wherein said memory cell stores an n-valued data (where n represents a positive integer not smaller than 3).

28. The device according to claim 26, wherein said memory cell is a non-volatile transistor having a floating gate, a control gate, a source and a drain; and

said write circuit supplies said write voltage to the control gate of said non-volatile transistor and said write control voltage to the drain of said non-volatile transistor.

29. A non-volatile semiconductor memory device comprising:

an electrically data rewritable non-volatile semiconductor memory cell; and

a write circuit configured to write data in said memory cell, said write circuit writes a data in said memory cell as a first step by supplying a sequentially stepwise increasing write voltage and a write control voltage having a first effective voltage level to said memory cell, continues the writing of said data in said memory cell by changing said write control voltage to a second effective voltage different from said first effective voltage in response to an advent of a first write state of said memory cell and inhibits any operation of writing a data to said memory cell in response to an advent of a second write state of said memory cell;

wherein the difference between said second effective voltage and said first effective voltage is selected so as to be greater than the increment of said write voltage.

30. The device according to claim 29, wherein said memory cell stores an n-valued data (where n represents a positive integer not smaller than 3).

31. The device according to claim 29, wherein said memory cell is a non-volatile transistor having a floating gate, a control gate, a source and a drain; and

said write circuit supplies said write voltage to

the control gate of said non-volatile transistor and said write control voltage to the drain of said non-volatile transistor.